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A CMOS pulse-shrinking delay element for time interval measurement

P Chen, SI Liu, J Wu - IEEE TRANSACTIONS ON CIRCUITS ..., 2000 - ieeexplore.ieee.org

... This circuit operates in current-mode and offers a simpler **circuit configuration** compared with its voltage-mode counterparts in [1]–[4], [16]. ... Norwell, MA: Kluwer, 1993. A CMOS Pulse-Shrinking Delay Element For Time Interval Measurement ...[Cited by 41](#) - Related articles - [SL Direct](#) - All 7 versions[ntu.edu.tw \[PDF\]](#)

Current-Mode All-Pass Filters Using Current Differencing Buffered Amplifier and a New High-Bandpass Filter Configuration

A Toker, S Ozoguz, O Cigekoglu, C ... - IEEE Transactions on ..., 2000 - ieeexplore.ieee.org

Page 1. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING, VOL. 47, NO. 9, SEPTEMBER 2000 949 [13] TH

Kuo, WC Wang, KD Chen, JR Chen, and JW Yeh, "Stabilizing ...

[Cited by 60](#) - Related articles - [SL Direct](#) - All 3 versions

Delay circuit having one of a plurality of delay lines which may be selected to provide an operation of a ring oscillator

JA Puisipher, RH Wolff, SG Worthington - US Patent 5,067,842, 1992 - Google Patents

... SUMMARY OF THE INVENTION 35 The invention is a delay **circuit configuration** that maintains the delay period near to a desired delay despite ... the reference circuit is a serial delay line of 50 elements; in the reference circuit the output of the final **delay element** (inverted) is ...[Cited by 21](#) - Related articles

Circuit configuration employing a compare unit for testing variably controlled delay units

BD McMinn, SC Horne - US Patent 5,570,294, 1996 - Google Patents

... 5,570,294 20 CIRCUIT CONFIGURATION EMPLOYING A COMPARE UNIT FOR TESTING VARIABLY CONTROLLED DELAY UNITS BACKGROUND OF THE INVENTION ... 2. Description of the Relevant Art An electrical **delay element** is typically associated with an output signal ...[Cited by 19](#) - Related articles

Feedforward linearisation of 950 MHz amplifiers

RD Stewart, FF Tsuburra - IEE Proceedings H Microwaves, ..., 1988 - ieeexplore.ieee.org

... Fig. 1 shows the feedforward **circuit configuration**. ... A two tone signal comprising frequencies, and if, is fed to the main amplifier via coupler C, which also feeds a small sample of this signal via **delay element** T, to coupler C,. The output of the main amplifier that now contains the ...[Cited by 28](#) - Related articles - All 7 versions

Single-electron logic device based on the binary decision diagram

N Asahi, M Akazawa, Y Ameriya - IEEE Transactions on ..., 1997 - ieeexplore.ieee.org

... node acts as a **delay element** that holds a messenger electron (a) (b) Fig. 5. NOT logic circuit: (a) **circuit configuration**, (b) simulation result for the operation; plotted are clock waveforms, input signal, and output (the terminal-node net charges normalized to the electron charge). ...[Cited by 83](#) - Related articles - [SL Direct](#) - All 3 versions

Delay clock generator for generating a plurality of delay clocks delaying the basic clock

K Wada, M Akiyama - US Patent 5,764,092, 1998 - Google Patents

... Only the selector 90 always selects output of nFTATI pin npirRTPTTON OF THF " the **delay element** 81' Consequently, when all delay control DE ... 6 is a detailed circuit diagram of the delay control 11 to In-respectively have the same **circuit configuration** as circuit 31. ...[Cited by 20](#) - Related articles

20-GHz 5-dB-Gain Analog Multipliers with AlGaAs/GaAs HBT's

K Osafune, Y Yamauchi - IEEE Transactions on Microwave ... , 1994 - ieeexplore.ieee.org

... i g: 2 T' | r - Fig. I. **Circuit configuration** of an analog multiplier. of the RF or IF and LO ports without baluns. ... 10 100 -10 LO Frequency (GHz) Fig. 6. GHz. PLO=PRF=-7.5 dBm. Conversion gain versus LO frequency; swept WF and fL0, fIF=OS **delay element**, is used. ...[Cited by 29](#) - Related articles - [SL Direct](#) - All 5 versions

Method for substantially eliminating hold time violations in implementing high speed logic circuits or the like

RA Price, BC Thielges - US Patent 5,259,006, 1993 - Google Patents

... steps of providing a synchronizer flip-flop device or latch corresponding to every flip-flop device or latch specified in the **circuit configuration** data. ... A **delay element** 26 is shown on the clock line 28 to ^b of each synchronizer 300, 306 before the user's illustrate the effect of skew ...[Cited by 54](#) - Related articles

Surface acoustic wave ultraviolet photodetectors using epitaxial ZnO multilayers grown on r-plane sapphire

NW Emanetoglu, J Zhu, Y Chen, J Zhong, Y ... - Applied physics ..., 2004 - link.springer.com

... A SAW UV detector was reported to cause a phase shift at when used as a **delay element** in the feedback path of an oscillator. ... at for a light power of is , corresponding to a frequency shift of in an oscillator circuit, calculated for the standard oscillator **circuit configuration** with the ...[tsinghua.edu.cn \[PDF\]](#)

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